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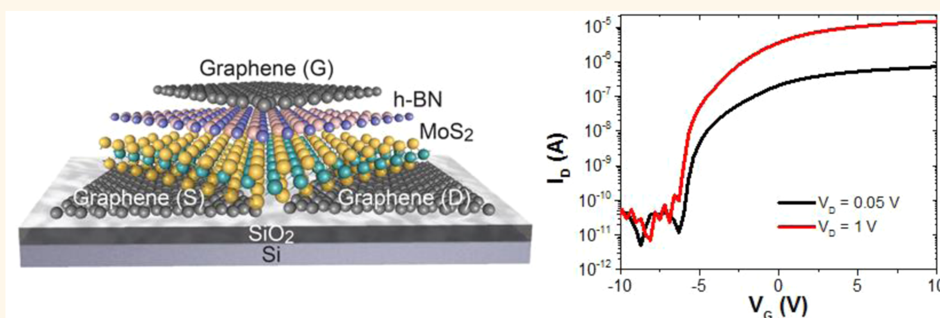
ARTICLE

Field-Effect Transistors Built from All Two-Dimensional Material Components

Tania Roy,[†,‡,§] Mahmut Tosun,[†,‡,§] Jeong Seuk Kang,[†,‡,§] Angada B. Sachid,[†] Sujay B. Desai,[†,‡,§] Mark Hettick,[†,‡,§] Chenming C. Hu,[†] and Ali Javey[†,‡,§,*]

[†]Electrical Engineering and Computer Sciences, University of California, Berkeley, California 94720, United States, [‡]Materials Sciences Division, Lawrence Berkeley National Laboratory, Berkeley, California 94720, United States, and [§]Berkeley Sensor and Actuator Center, University of California, Berkeley, California 94720, United States

ABSTRACT



We demonstrate field-effect transistors using heterogeneously stacked two-dimensional materials for all of the components, including the semiconductor, insulator, and metal layers. Specifically, MoS_2 is used as the active channel material, hexagonal-BN as the top-gate dielectric, and graphene as the source/drain and the top-gate contacts. This transistor exhibits n-type behavior with an ON/OFF current ratio of $>10^6$, and an electron mobility of $\sim$33 $cm^2/V \cdot s$. Uniquely, the mobility does not degrade at high gate voltages, presenting an important advantage over conventional Si transistors where enhanced surface roughness scattering severely reduces carrier mobilities at high gate-fields. A WSe_2—MoS_2 diode with graphene contacts is also demonstrated. The diode exhibits excellent rectification behavior and a low reverse bias current, suggesting high quality interfaces between the stacked layers. In this work, all interfaces are based on van der Waals bonding, presenting a unique device architecture where crystalline, layered materials with atomically uniform thicknesses are stacked on demand, without the lattice parameter constraints. The results demonstrate the promise of using an all-layered material system for future electronic applications.

KEYWORDS: layered materials · transition metal dichalcogenides · graphene · hexagonal boron nitride · MoS_2 · heterolayers

Two-dimensional (2-D) material systems have aroused immense interest in research due to the possibility of obtaining thickness uniformity down to a monolayer without surface dangling bonds. Graphene (Gr), as a two-dimensional semimetal has been studied extensively for the purpose of analog and digital applications. However, the absence of an intrinsic bandgap in Gr overshadows its attractive properties of small quantum capacitance and extremely high mobilities in scaled transistors.[1−3] Transition metal dichalcogenides (TMDC), with an inherent bandgap, tunable by composition and the number of layers, have ignited significant interest and promise over the past few years for both electronic and optoelectronic applications.[4−7] For instance, MoS_2 and WSe_2 have been used to obtain excellent switching current ratios (up to 10^8), and ideal subthreshold slope (60 mV/decade).[8−12] One of the primary advantages of layered materials is, in principle, the absence of dangling bonds, which rules out performance degradation due to interface states.[13] Uniquely, heterostructures using two-dimensional materials would not suffer from constraints of lattice mismatch. A layered material can be seamlessly transferred onto another, and bond by van der Waal's (vdW) forces, leaving the interface pristine. An ideal transistor structure would, therefore, be composed of a TMDC material as the channel, with a

* Address correspondence to ajavey@eecs.berkeley.edu.

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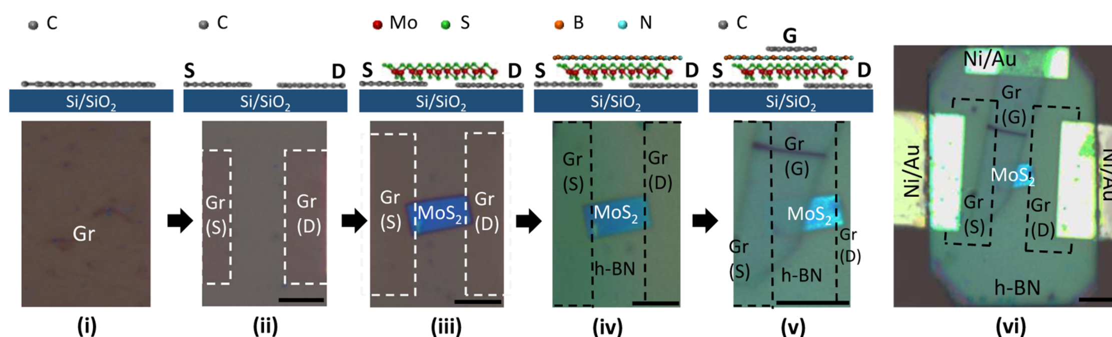

Figure 1. Schematics (not to scale) of the fabrication process steps (top) and the corresponding optical microscope images (bottom) of a representative all-2D FET. (i) Transfer of large-area CVD grown bilayer graphene onto a Si/SiO_2 substrate. (ii) Bilayer graphene patterning by O_2 plasma to define S/D contacts. (iii) Transfer of a few-layer MoS_2 flake on top of the patterned grahene S/D contacts. (iv) Transfer of a few-layer h-BN gate dielectric, overlapping the MoS_2 channel. (v) Transfer of a multilayer graphene top gate electrode. (vi) Optical microscope image of a fully fabricated all-2D transistor. Scale bar is 5 μm for all images.

layered insulator as the gate dielectric, and layered metallic source/drain and gate contacts. Atomically thin p-n diodes have been reported, using MoS_2 and WSe_2 monolayers as the electron and hole conducting layers, respectively.[14−16] These vdW heterostructure diodes have exhibited excellent rectification behavior owing to the abruptness of the 2D−2D interface, with ideality factor of 1.2. MoS_2 transistors with graphene source/drain contacts have been used to fabricate flexible, transparent transistors.[17] Also, flexible and transparent MoS_2 transistors with graphene source/drain contacts were fabricated with h-BN as back gate dielectric, demonstrating negligible hysteresis in transport characteristics.[18] Heterostructures with 2D materials have been used for memory applications and tunnel transistors. Gr/MoS_2 heterostructures have been used for nonvolatile memory cells.[19] Tunnel transistors fabricated with Gr/hexagonal-BN (h-BN)/Gr and Gr/MoS_2/Gr open the prospect of obtaining steep transistors with such an architecture.[20] Vertical Gr/h-BN/Gr heterostacks have also exhibited negative differential resistance, allowing the prospect of vdW heterostructures in analog electronics.[21] Gr/WS_2/Gr heterostructures have demonstrated strong light-matter interactions, leading to enhanced photon absorption and electron−hole creation.[22] This has opened the possibility of flexible photovoltaic devices with layered 2D materials. Heterobilayers of WSe_2 and MoS_2 have shown strong interlayer coupling with spatially direct absorption and spatially indirect emission, exhibiting yet another unique property of TMDC heterostructures. TMDC heterojunctions with III−V, Si, and carbon nanotubes have also been explored previously, demonstrating electrically active vdW interfaces built from highly dissimilar semiconductors.[23−26] However, a transistor made completely from two-dimensional materials to leverage the absence of interface states with digitally controlled and atomically uniform thickness has not been reported so far. In this work, we use large area chemical vapor deposited (CVD) Gr to contact few-layer MoS_2 crystals. We use exfoliated hexagonal boron nitride as the layered gate dielectric and exfoliated Gr as the top-gate contact. The resulting field-effect transistor (FET) made completely of layered materials exhibits a high ON/OFF current ratio of $>10^6$, with a MoS_2 electron mobility of 33 $cm^2/V \cdot s$. We also demonstrate the rectification behavior of an all-2D diode, using MoS_2−WSe_2 heterojunction contacted with Gr as the source/drain electrodes.

Figure 1 shows the fabrication steps and corresponding optical images of a representative all-2D FET. The details of the process are as follows. CVD grown bilayer or monolayer Gr on a Cu foil was coated with PMMA. The PMMA-coated substrate was treated with dilute HNO_3 and the Cu was etched by inserting the foil into an ammonium persulfate solution bath for 18 h. After the Cu foil was completely etched away, the floating PMMA coated Gr was scooped out of the bath and transferred onto a Si/SiO_2 (260 nm) substrate (Figure 1(i)). The sample was baked at 220 °C for 5 min to improve Gr adhesion on the SiO_2 surface followed by PMMA removal using acetone.[27,28] Ni/Au (30 nm/30 nm) bond pads were then formed by electron-beam (e-beam) lithography, evaporation and resist lift-off. Gr was subsequently patterned using e-beam lithography and oxygen plasma etching to define the S/D electrodes of the FET (Figure 1(ii)). MoS_2, h-BN, and Gr multilayers as the active channel, gate dielectric, and the gate electrode, respectively, were sequentially stacked on the Gr S/D contacts using a pick and transfer process. Specifically, MoS_2, h-BN and Gr multilayers were first exfoliated onto Si/SiO_2 process substrates. Flakes of interest were patterned into rectangular shapes with desired dimensions using electron-beam lithography and dry etching. MoS_2 and h-BN were etched using XeF_2, and Gr was etched using O_2 plasma. The substrates were then spin coated with PMMA (6 μm in thickness). PMMA was used as a carrier layer to pick the flake of interest off the substrate, and to

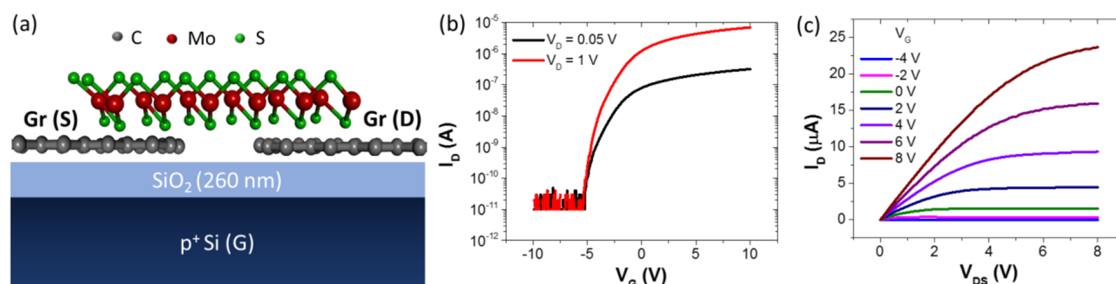

Figure 2. Back-gated few-layer MoS_2 FET with monolayer graphene contacts. The p^+ Si substrate is used as the back-gate. (a) Device schematic (not to scale). (b) I_D-V_G curves at different V_D. (c) I_D-V_D characteristics.

dry-transfer onto the device substrate. First, using an engraver, the PMMA slab around the patterned flake of interest was cut under an optical microscope. The slab was poked from all sides to release from the SiO_2 substrate. The PMMA slab with the flake was then picked with a needle under a microscope, and transferred onto the targeted area on the device substrate. The sample was subsequently annealed at 180 °C for 2 min after each transfer step to improve the adhesion of the transferred flakes to the substrate. The PMMA carrier layer was removed by immersion in dichloromethane after each transfer step. With this dry transfer method, a MoS_2 flake was transferred in between the prepatterned Gr S/D contacts (overlapping each Gr contact) to form the active channel (Figure 1(iii)). A h-BN flake was then dry-transferred onto the MoS_2 channel area to form the gate dielectric (Figure 1(iv)) followed by the transfer of a multilayer Gr flake to form the top-gate contact (Figure 1(v)). The device was annealed in forming gas (5% H_2, 95% N_2) for 3 h at 200 °C in order to improve the interface properties. An optical image of a fully fabricated FET is shown in Figure 1(vi). Note that the alignment accuracy for this manual pick and transfer process is ~2 μm. In fact, for the specific device shown in Figure 1, there is ~2 μm misalignment between the Gr gate and S/D electrodes. This results in a gate underlapped MoS_2 region which contributes to the parasitic resistance of the device, but otherwise does not restrict the switching behavior. In principle, the alignment accuracy and yield can be improved in the future by using an automated pick and transfer process. MoS_2/WSe_2 heterojunction diodes with Gr contacts were also fabricated using a similar transfer approach, except that MoS_2 and WSe_2 layers were sequentially transferred such that each flake is in contact with only one prepatterned Gr electrode, with a MoS_2/WSe_2 overlap region in the middle of the device. All electrical measurements were performed at room temperature, in ambient air.

RESULTS AND DISCUSSION

We first examine the properties of Gr contacted MoS_2 back-gated FETs (Figure 2a). Figure 2b,c shows the I_D-V_G and I_D-V_D characteristics of a representative MoS_2 transistor with Gr S/D contacts. Here the p^+Si/SiO_2 (260 nm) substrate is used as the back gate. The channel length, L, and width, W, are ~7 μm and ~25 μm, respectively. This MoS_2 transistor with vdW Gr contacts exhibits clear n-type characteristic with ON/OFF current ratio of ~10^6. Notably, the low V_{DS} regime of the output characteristics (Figure 2b) is linear without an inflection point. This result suggests that Gr provides efficient contacts to the conduction band of MoS_2 for electron injection. This observation is similar to those previously reported for MoS_2 devices with elemental metal contacts, where the FETs exhibited n-type characteristics. We have also characterized Gr contacted WSe_2 multilayer devices. In contrast to MoS_2 devices, Gr contacted WSe_2 FETs exhibit a p-type characteristic with nonlinear I_D-V_D curves arising from a large Schottky barrier (SB) height to the valence band of WSe_2 at the Gr interface (Supporting Information, Figure S1). The results suggest that the workfunction of Gr, which is ~4.5 eV based on literature,[29] is low enough for contacting electrons in MoS_2, but not high enough to form an ohmic contact to holes in WSe_2. Given the ability to chemically dope Gr,[30] in the future, it should be possible to explore Gr with tuned work function to further improve the contact resistances to both MoS_2 and WSe_2. This presents potentially a unique feature of Gr contacts over elemental metals.

Next we fabricated an all-2D transistor, where a MoS_2 flake (thickness, ~10 nm) is contacted by bilayer Gr S/D, with h-BN (thickness, ~55 nm) as the top-gate dielectric and multilayer Gr (thickness, ~10 nm) as the top-gate electrode (Figure 3a). In this system, all interfaces are based on vdW bonding, presenting a unique device architecture where crystalline, layered materials are stacked on demand, without the lattice parameter constraints. The device has a channel length and width of ~3 and 2.7 μm, respectively. Panels b and c of Figure 3 depict the transfer and output characteristics of this all 2-D FET, respectively. The device demonstrates clear n-type switching behavior, with ON/OFF current ratio of >10^6 (the OFF current being limited by the noise level of the system).

The contact resistance of TMDC devices is generally significant as compared to the channel resistance. Thus, in order to properly extract the device mobility, the contact resistances must be carefully taken into

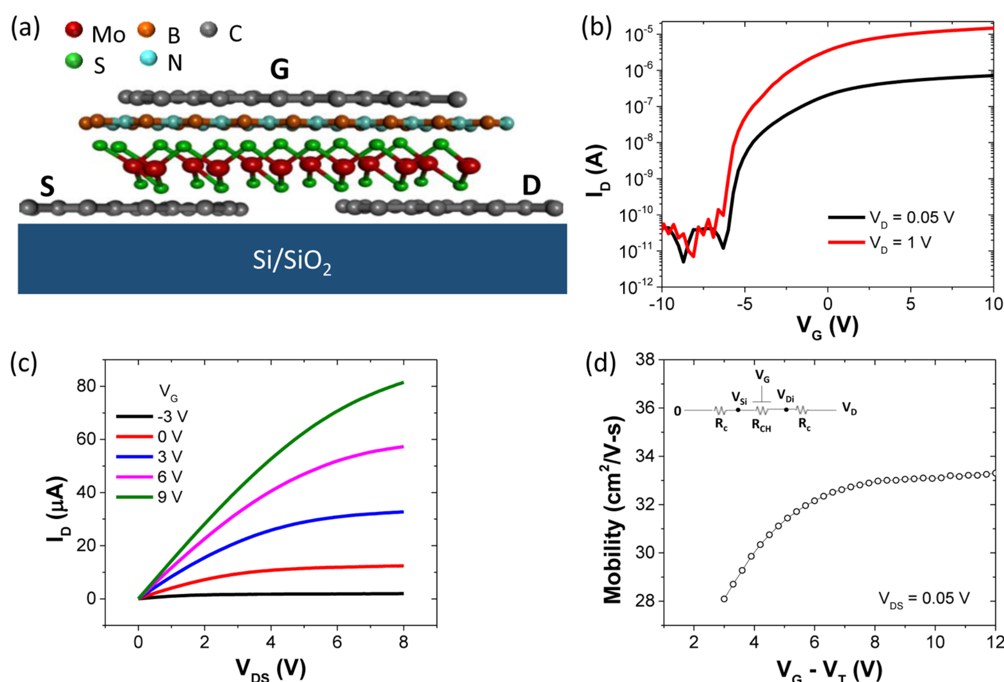

Figure 3. All-2D MoS_2 FET with few-layer h-BN gate dielectric, and bilayer graphene source/drain and multilayer graphene top-gate electrodes. (a) Device schematic (not to scale). (b) I_D-V_G characteristics at different V_D. (c) I_D-V_D characteristics. (d) Extracted mobility as a function of gate voltage, $V_G - V_t$. The inset shows the circuit model of the device used for mobility extraction. The substrate is grounded during all measurements.

account. To extract the mobility of the all-2D FET, we used a model described as follows. The potential from the source to the drain is assumed to drop across three resistors in series, as shown in the inset of Figure 3d: the source and drain contacts, R_c, and the active channel, R_{CH}. The drain current, I_D can be expressed as $I_D = \mu C_{ox}(W/L)(V_{G-i} - V_t)(V_{D-i})$, where μ is the mobility, C_{ox} is the capacitance of the gate oxide, W and L are the channel width and length, respectively, V_t is the threshold voltage, and V_{G-i} and V_{D-i} are the intrinsic gate and drain voltages after subtracting the potential drops across the source and drain contact resistances. The channel resistance R_{CH} can be then defined as $R_{CH} = V_{D-i}/I_D = L/(\mu C_{ox}W(V_{G-i} - V_t))$. The total resistance between the source and the drain is given by $R_{total} = R_{CH} + 2R_c = V_D/I_D = L/(\mu C_{ox}W(V_{G-i} - V_t)) + 2R_c$. At high $V_{G-i} - V_t$, the channel resistance becomes negligible with the total resistance being dominated by the contacts. That is $R_{total} \approx 2R_c$. From the measured transfer curves at high V_G and $V_D = 0.05$ V, we extract $R_c \sim 15$ kΩ (see Supporting Information for details). I_D can be expressed as $\mu C_{ox}(W/L)(V_G - V_t - I_D R_c)(V_D - 2I_D R_c)$. Assuming h-BN has a dielectric constant of 4, C_{ox} is calculated to be $\sim 6.4 \times 10^{-8}$ F/cm^2. The extracted electron mobility for our all-2D device is subsequently calculated as a function of $V_G - V_t$ as shown in Figure 3d. The peak mobility is ~ 33 cm^2/V·s which is consistent with the range of electron mobility values reported in the literature for MoS_2 FETs.[8,31] We also calculate the field-effect mobility μ_{FE} using the expression $\mu_{FE} = dI_D/dV_G(L/WC_{ox}V_{DS})$, at $V_{DS} = 0.05$ V. In this method, the contact resistance is not corrected for, and the mobility is extracted to be 26 cm^2/V·s, which is slightly lower than the value obtained when the contact resistance is corrected for.

Notably, in distinct contrast to conventional Si MOSFETs, the mobility of the all-2D FET does not decrease at high gate fields, and remains rather constant (Figure 3d). This observation is highly desirable for FET operation since it reduces the V_G dependence of the ON-state device performance (*e.g.*, speed), thus making the eventual circuit design based on the demonstrated device architecture more robust. In conventional Si MOSFETs, the mobility drastically decays at high gate fields as the carriers are moved closer to the device surface, thereby making them more susceptible to surface roughness scattering.[32] In contrast, in the all-2D FET, the impact of surface roughness scattering of carriers is expected to be less severe given the vdW nature of the bonds with atomically uniform thicknesses of the semiconductor channel and the gate dielectric. In addition, given the 2D nature of the thin MoS_2 layers used, the charge centroid of carriers is expected to be near the middle of the MoS_2 thickness with minimal dependence on the gate fields. This was previously observed in ultrathin InAs and WSe_2 FETs.[33,9] These two effects contribute to the lack of gate dependence in mobility at high gate fields, and demonstrate an important advantage of the all-2D FET.

Finally, we demonstrate an all-2D diode using WSe_2 as the hole conducting layer, MoS_2 as the electron conducting layer, and Gr as the contacts (Figure 4a).

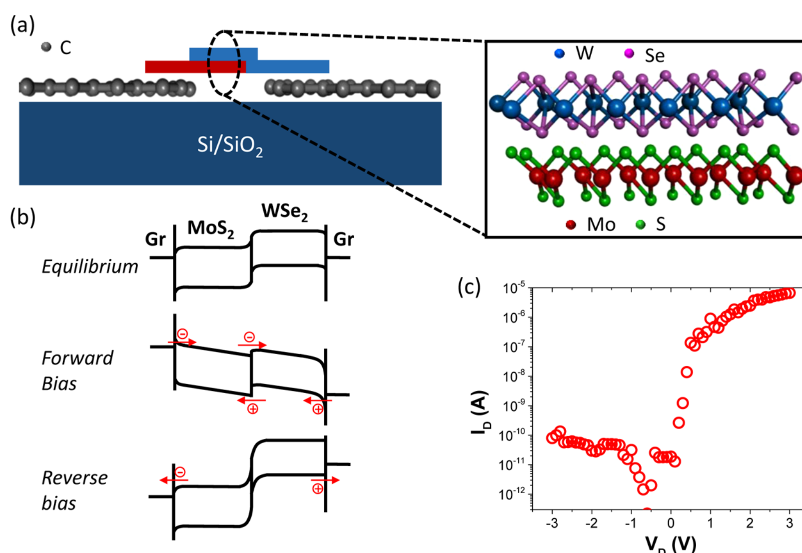

Figure 4. All-2D diode consisting of few-layer MoS_2 and WSe_2 as electron and hole conducting layers, respectively, and monolayer graphene as the electrical contacts. (a) Cross-sectional schematic of the diode (not to scale). (b) Qualitative band diagrams of the diode at equilibrium (V = 0 V), forward bias, and reverse bias. (c) Diode $I-V$ characteristics. The substrate was grounded during measurements.

As noted before, Gr forms a low resistance contact to the conduction band of MoS_2 for electron injection, but a Schottky contact to the WSe_2 valence band for hole injection. Thus, a Gr/WSe_2/MoS_2/Gr heterostructure is composed of a Schottky diode between Gr and WSe_2, and a heterojunction diode between WSe_2 and MoS_2. The band alignment for a WSe_2/MoS_2 heterobilayer was previously explored, showing a ~100 meV offset in the conduction band edge of the two materials.[15] Assuming a similar band offset for the multilayer heterojunction explored here, a qualitative band diagram can be drawn as shown in Figure 4b. Under forward bias, electrons from MoS_2 can cross the low barrier into WSe_2 and recombine with the holes that are injected from Gr into WSe_2. $I-V$ is determined by the MoS_2/WSe_2 junction, and the parasitic resistances of the Schottky contacts and the MoS_2 and WSe_2 films. Under reverse bias, the applied voltage is dropped at the MoS_2/WSe_2 junction and the current is limited by the thermally generated electrons and holes. The measured diode characteristic is shown in Figure 4c. The device exhibits clear rectification behavior, with the forward bias current at 3 V being ~10^5 times larger than the reverse bias current. The diode ideality factor is extracted to be 1.4. The low reverse bias current and the ideality factor suggest high interface quality between MoS_2 and WSe_2 with minimal interface recombination/generation of carriers. This diode presents yet another example of configuring different layered material components into a functional device through the multistep transfer process.

CONCLUSIONS

In summary, we have demonstrated the operation of an all-2D transistor, using a TMDC channel material, h-BN gate dielectric, and graphene source/drain and gate contacts. This work presents a unique platform for utilizing heterostructures of user-defined layered materials with atomically uniform and digitally controlled thicknesses for functional devices. Importantly, the vdW bonding of the interfaces and the use of the multistep transfer process provide pathways for making complex devices based on crystalline layers without the constraints of lattice parameters. Future work involves thickness scaling of individual components down to a monolayer and channel length scaling down to the molecular-scale dimensions.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: Characteristics of back-gated WSe_2 p-FETs with graphene contacts; contact resistance calculations; Raman spectra of the all-2D FET; optical microscope image of the MoS_2/WSe_2 diode. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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